

Application No.: 09/550,282
Art Unit 2871

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REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-25 are now present in this application. Claims 1, 15 and 22 are independent.

Claims 1, 15, and 22 have been amended. Reconsideration of this application, as amended, is respectfully requested.

Reasons for Entry of Amendments

At the outset, it is respectfully requested that this Amendment be entered into the Official File in view of the fact that the amendments to the claims automatically place the application in condition for allowance.

In the alternative, if the Examiner does not agree that this application is in condition for allowance, it is respectfully requested that this Amendment be entered for the purpose of appeal. This Amendment was not presented at an earlier date in view of the fact that Applicants did not fully appreciate the Examiner's position until the Final Office Action was reviewed.

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Rejections under 35 U.S.C. § 103

Claims 1-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,172,728 to Hiraishi, in view of Applicants' disclosed Related Art and U.S. Patent No. 6,100,954 to Kim et al. (Kim). This rejection is respectfully traversed.

At the outset, Applicants assert that no admission of Prior Art in the Applicants' disclosure has been made.

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the instant application, Applicants respectfully submit that independent claims 1, 15 and 22 have been amended to recite a combination of elements in a liquid crystal display or a method of manufacturing a liquid crystal display, including a gate line formed on a transparent substrate, edges of said gate line being substantially straight and even, and a data line crossing said gate line and formed on said transparent substrate, edges of said data line being substantially straight and even. Applicants respectfully submit that this combination of elements as set forth in independent claims 1, 15 and 22 is not disclosed or made obvious by the prior art of record, including Hiraishi.

Hiraishi discloses a reflective liquid crystal display device including a plurality of scanning lines and a plurality of signal lines disposed so as to intersect with the plurality of scanning lines, wherein at least one of the

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scanning lines or the signal lines have at least one of bends, notches, protrusions and holes (see Hiraishi, Col.2, lines 37-48). By forming the scanning lines or the signal lines with uneven surfaces (particularly edge surfaces) as seen in all of the figures, Hiraishi asserts that the parasitic capacitance between the lines and the pixels is reduced, thereby preventing deterioration of the display quality. Hiraishi further asserts that by randomly patterning the signal lines, the parasitic capacitance caused between the signal lines and the pixel electrodes may be slightly different for each pixel. Thus, display unevenness caused by the offset of blocks for stepper exposures is prevented. Moreover, the non-uniform wavelength characteristics at the periphery of the pixel electrodes are minimized, thereby eliminating the influence of the light interference (see Hiraishi, Col.2, lines 48-58).

Clearly, gate and/or data lines having uneven edges is a key feature of the Hiraishi device. It is also quite clear that Hiraishi teaches away from edges of said gate line or data line being substantially straight and even. Accordingly, Hiraishi teaches away from Applicants' claimed invention.

As the Examiner must appreciate, a prior art reference that teaches away from the claimed invention is a significant factor to be considered in determining obviousness. A prior art reference must be considered in its entirety, as a whole, including portions that would lead away from the claimed invention. Particularly, Hiraishi fails to disclose or suggest edges of said gate line being substantially

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straight and even or edges of said data line being substantially straight and even, as recited in independent claim 1 (as amended), and similarly stated in independent claims 15 and 22 (as amended). Neither Kim, nor the Applicants' related art can fill this vacancy, which is clearly contrary to the express teachings of Hiraishi.

Claims 2-14, 16-21 and 23-25 depend, either directly or indirectly on independent claims 1, 15, and 22. Since neither Hiraishi, nor Kim, nor Applicants' disclosed related art discloses or suggests the above-recited features of independent claims 1, 15 and 22, Hiraishi, in view Kim and the related art cannot render claims 1-25 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

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If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

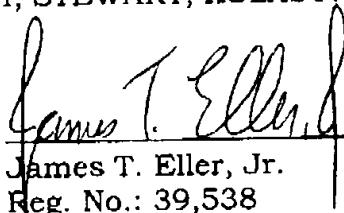
Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

1. (Twice Amended) A liquid crystal display (LCD), comprising:
 - a gate line formed on a transparent substrate, edges of said gate line being substantially straight and even [having a gate electrode connected thereto];
 - a data line crossing said gate line and formed on said transparent substrate, edges of said data line being substantially straight and even;
 - an insulating layer electrically insulating said data line from said gate line;
 - a thin film transistor formed at an intersection of said gate line and said data line, and connected to said gate line and said data line;
 - a passivation layer formed over the thin film transistor;
 - a pixel electrode formed on the surface of the passivation layer[, but not over said gate electrode to act as a light shielding layer therefor, said pixel electrode providing a gap space over said data line so as not to shield light therefrom]; and
 - a low reflective layer formed on at least a portion of at least one of said gate line and said data line[, said data line having no light shielding layer formed thereover].

15. (Twice Amended) A method of manufacturing a liquid crystal display, comprising:

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forming a gate line and a portion protruding from said gate line to serve as a gate electrode of a thin film transistor on a transparent substrate, edges of said gate line being substantially straight and even;

forming an insulating layer electrically insulating said gate line;

forming a data line over said transparent substrate and crossing said gate line, edges of said data line being substantially straight and even;

forming a passivation layer over the thin film transistor;

forming a pixel electrode on the surface of the passivation layer[, but not over said gate electrode to act as a light shielding layer therefor, said pixel electrode providing a gap space over said data line so as not to shield light therefrom]; and

first forming a low reflective layer over at least a portion of at least one of said gate line and said data line[, said data line having no light shielding layer formed thereover].

22. (Twice Amended) A method of manufacturing a liquid crystal display, comprising:

forming a gate line and gate electrode connected thereto on a transparent substrate, edges of said gate line being substantially straight and even;

forming an insulating layer over said gate line and gate electrode;

forming a semiconductor layer over said gate electrode;

forming a data line crossing said gate line, edges of said data line being substantially straight and even, a source electrode connected to said data line and on a first portion of said semiconductor layer, and a drain electrode on second portion of said semiconductor layer;

forming a low reflective layer over at least a portion of at least one of said gate line and said data line[, said data line having no light shielding layer formed thereover];

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forming a passivation layer having a contact hole exposing said drain electrode over said transparent substrate; and
forming a pixel electrode on said passivation layer [but not over said gate electrode to act as a light shielding layer therefor, said pixel electrode providing a gap space over said data line so as not to shield light therefrom] and connected to said drain electrode via said contact hole.